



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1459  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,918	11/14/2003	Mitsuyoshi Mori	60188-710	7667
<div>7590 12/21/2007</div> <div>Jack Q. Lever, Jr. McDERMOTT, WILL &amp; EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096</div>				
EXAMINER				
INGHAM, JOHN C				
ART UNIT		PAPER NUMBER		
2814				
MAIL DATE		DELIVERY MODE		
12/21/2007		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/706,918

**Applicant(s)**

MORI ET AL.

**Examiner**

JOHN C. INGHAM

**Art Unit**

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 34-37, 39-48, 66 and 68-71 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 34-37, 39, 42-48, 66, 68 and 69 is/are rejected.
- 7) ☒ Claim(s) 40, 41, 70 and 71 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-848)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 12/21/06; 9/24/07
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 September 2007 has been entered.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on 21 December 2006 has been considered.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims **34-37, 39, 42-47 and 68** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (US 6,352,869) and Wong (US 5,708,263).

5. Regarding claims **34-35, 39, 42 and 44**, the '869 patent discloses in Figure 3B a solid state imaging apparatus comprising: a plurality of photoelectric conversion cells (2x2 pixels are shown out of the matrix, where the two rows shown correspond to the second and third rows as described in the instant application in Fig 1), each including a plurality of photoelectric sections of photodiodes arranged in a matrix including at least first (Fig 3B item 2) and second (Fig 3B next adjacent row to item 2, not shown) rows and first and second columns (Fig 3B items 3 and 4); a plurality of first floating diffusion sections (41 shared between adjacent row and column pixels) provided between said photoelectric conversion cells, each being shared by, and being connected to, the photoelectric sections (71-74) which are included in the first row of each photoelectric conversion cell via a plurality of transfer transistors (TG), respectively; a plurality of second floating diffusion sections (in the next adjacent row to row 2, but not shown) each being shared by, and being connected to the photoelectric sections which are included in the second row of each photoelectric conversion cell via a plurality of transfer transistors, respectively; a plurality of read-out lines (col 2 In 24-28) each being selectively connected to the transfer transistors (TG1 and other transistors on pixels in the same row, or TG2 and other transistors on pixels in the same row) connected to the photoelectric conversion sections which are included in one of the first and second columns; a plurality of first pixel amplifier transistors (32) coupled to and detecting and outputting the potential of each first floating diffusion section; a plurality of second pixel amplifier transistors (in the next row not shown) coupled to and detecting and outputting

the potential of each second floating diffusion section, wherein the first and second pixel amplifiers comprises a source follower transistor (col 2 ln 26).

The '869 patent shows that four adjacent row and column pixels share the floating diffusion regions and amplifier between them. Another cell adjacent to the one shown will include another shared amplifier and another shared floating diffusion. This cell structure is the same as that claimed in the instant application and shown in Fig 4, where row 1 of the '869 patent corresponds to the third row in Fig 1, and row 2 of the '869 patent corresponds to the second row in Fig 1. A cell can be defined as four adjacent pixels (in the row and column direction) sharing a common diffusion and common amplifier, or can be defined as two adjacent pixels (in the row or column direction) sharing a floating diffusion and amplifier and another two adjacent pixels sharing another floating diffusion and amplifier.

The '869 patent does not specify wherein the plurality of read-out lines are each selectively connected to the transfer transistors that are not included in the same row, or wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read out lines. Instead the '869 patent shows each cell having its own read out line.

Wong teaches in Fig 1A wherein the read out lines are commonly connected to four transfer transistors (TX items 26, 46, 66, 86) in two rows and two columns in order to read out the photodetectors with fewer devices and reduced noise (col 1 ln 9-13). It would have been obvious to one of ordinary skill in the art at the time of the invention to

use the teachings of Wong in the device disclosed by the '869 patent in order to read the photodetectors with fewer devices and reduced noise.

6. Regarding claim **36**, the '869 patent discloses the apparatus of claim 39, wherein the plurality of read lines are connected to a vertical scanning circuit (col 2 ln 19, each row is read at a time, therefore the array is scanned vertically). Wong also discloses that rows are read out at a time (col 3 ln 38-45).

7. Regarding claims **37 and 43**, the '869 patent discloses the apparatus of claim 39, wherein a plurality of a pair of signal lines (one shown, column output buss) outputs signals from the first pixel amplifier (32) and the second pixel amplifier (not shown, in an adjacent column) to the outside, wherein a select transistor (34) is provided between the pixel amplifier transistor and the signal line to selectively conduct between the pixel amplifier and the signal line.

8. Regarding claims **45**, the '869 patent discloses the apparatus of claims 39 and 49, further comprising a reset transistor (36), wherein the drain of the reset transistor is connected to the drain of the pixel amplifier transistor (both connect to node VDD) so that a drain is shared by the reset transistor and the pixel amplifier transistor.

9. Regarding claims **46**, the '869 patent discloses in Fig 3A the apparatus of claims 39 and 49, wherein the photoelectric conversion sections are arranged so as to be spaced apart from one another by a certain distance in the row direction .

10. Regarding claims **47**, the '869 patent discloses in the apparatus of claims 39 and 49, further comprising a signal processing circuit (bottom dotted outline circles) for processing an output signal from each pixel amplifier transistor (32).

11. Regarding claim **68**, the '869 patent discloses in Fig 3B the apparatus of claim 39, wherein respective charges of the photoelectric conversion sections (PD) each connected to one of the read-out lines and being read out by the transfer transistors (TG) are read out by said first floating diffusion section (FD).

12. Claim **48** is rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent, Wong and Yamazaki (US 2002/0145582). The '869 patent and Wong disclose the apparatus of claim 39, but do not specify wherein the photoelectric conversion cells are separated from one another by a power supply line which also functions as a light-shielding film.

Yamazaki teaches the use of a power supply line between pixels which is also used as a light shield in order to protect the channel formation regions and p type semiconductor regions (¶ 90). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yamazaki on the structure of the '869 patent and Wong in order to use the power supply line as a light shield for channel and p type regions between pixels or pixel sections.

13. Claims **66 and 69** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '869 patent, Wong and Patterson (US 6,541,794).

14. Regarding claim **66**, the '869 patent and Wong disclose each limitation as claimed in claim 39 except for disclosing that the solid state imaging apparatus is part of a camera. Patterson teaches that arrays of photoactive pixel circuits are used in

cameras (col 1 ln 11) since they are suitable for capturing images projected onto the arrays (col 1 ln 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Patterson on the array disclosed by the '869 patent and Wong in order to capture images.

15. Regarding claim **69**, the '869 patent discloses in Fig 3B the apparatus of claim 66, wherein respective charges of the photoelectric conversion sections (PD1) each connected to one of the read-out lines and being read out by the transfer transistors (TG1) are read out by said first floating diffusion section (FD).

***Allowable Subject Matter***

16. Claims **40, 41, 70 and 71** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose or make obvious the apparatus of claim 39 wherein in each photoelectric conversion cell, a first read-out line is connected to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the first column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the second column. The prior art also does not disclose or make obvious the device of claim 39, wherein in each photoelectric conversion cell, a first read-out line is connected



to a gate of a transfer transistor included in the first row and the first column and a gate of a transfer transistor included in the second row and the second column, and a second read-out line is connected to a gate of a transfer transistor included in the first row and the second column and a gate of a transfer transistor included in the second row and the first column. Finally the prior art does not disclose or make obvious the device as claimed in claims 70 and 71, wherein only two read out lines are disposed within the photoelectric conversion cells.

### ***Response to Arguments***

18. Applicant's arguments with respect to claims 34-37, 39-48, 66 and 68-71 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/  
Primary Examiner  
Art Unit 2814

John C Ingham  
Examiner  
Art Unit 2814

/J. C. I./  
Examiner, Art Unit 2814